

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

1.Description

Designed and engineered to accommodate customers high usage 2000 cycles at 0°C to 85°C, the loopback module series supports 100G/400G/800G Ethernet, InfiniBand and Fiber Channel applications. Software defined multiple power consumption may emulate the optical module power, and the embedded insertion loss characteristics emulate the real-world cabling environment. The built-in surge current mitigation technology mitigates DUT risks from being damaged. The broad operating temperature range accommodates enterprise, datacom and telecom applications. The loopback module may be used for port testing, field deployment testing and equipment troubleshooting.

2.Features

- Hot-pluggable 800G OSFP Active Loopback
- 3nm CMOS process DSP
- Compliant with OSFP MSA, close top
- VCC voltage ranges from 2.97V to 3.63V
- Operating case temperature 0°C to +85 °C
- Multi-color LED on the front
- The module power distributed to the 5 burners
- Customized CMIS Rev 5.2

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3.Production Description

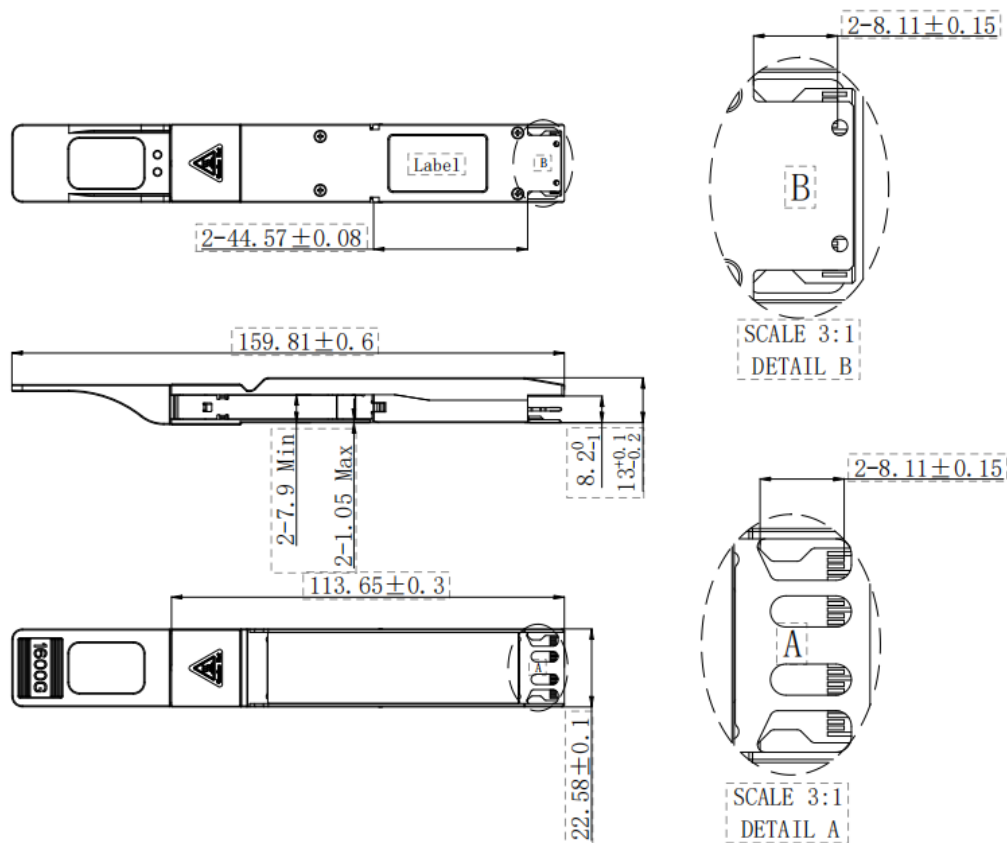
3.1 Product Name And Series Number(s)

800G Active Loopback Module

JPC P/N	Bit Rate	Function	Connector	Display
P69**LKKSX00-1	800G	Active Loopback	NA	Multi-color LED

Notes : ** Indicates the customer code.

3.2 Dimension, Materials, Plating and Marking



Mechanical Package Outline (All dimensions in mm)

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
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3.3 OSFP module dimension

Spec (mm)	Critical	Description
22.58±0.10	Y	Width of module, overall
12.95±0.15	Y	Height of module
1.0±0.1	Y	PCB thickness (measured over pads)
18.77±0.07	Y	PCB Lead-in width
113.65±0.3	Y	Body length (End to End), Type 1
159.81±0.6	Y	Body length (End to End), Type 2
7.9	Y	Height, max. above module
1.05	Y	Height max. below module
44.57±0.8	Y	PCB position (vertical) (Distance from bottom of Module to center of PCB)
<u>2</u> X 45° <u>MAX</u>	Y	PCB, end chamfer (top and bottom)
69.8 minimum	Y	Envelope dimension from datum B
C0.25±0.08 X 45°	Y	PCB, end chamfer (side corners)
Flatness		0.05mm
usability	Y	No snag, sharps that would prevent mechanical function
label	Y	Recessed below external surface, cannot peel off. No labels on heatsink surface
Module insertion/extraction	Y	Insertion = 40N (max), extraction = 30N (max)
Latch function	Y	Able to insert, wiggle, and extract
Roughness	Y	0.8Ra

4. Application and Standard

- Switch aging and testing
- 8x100G, 8x50G ,8x25G active loopback
- OSFP port/system testing

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- Support IEEE 802.3cd / 802.3bs / 802.3ck
- Compliant with OSFP Rev 3.0 and CMIS Rev 4.0

5.Product Specification

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings				
Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{cc}	-0.3	3.6	V
Storage Temperature	T _s	0	+85	°C
Operating Humidity	RH	5	+85	%
Control Input Voltage	V _I	-0.3	V _{CC} +0.3	V

5.2 Recommended Operating Conditions

Recommended Operating Conditions					
Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T _C	0	-	85	°C
Power Supply Voltage	V _{cc}	2.97	3.3	3.63	V
Power Dissipation	P _{diss}	-	-	32	W
Supply Current	I _{cc}	1.5	-	10.8	A

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5.3 High Speed Characteristics

High Speed Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	degC	Temperature range 0 to 85°C
Temperature monitor absolute error	DMI_VCC	-10%		10%	V	Voltage range 2.97 to 3.63V

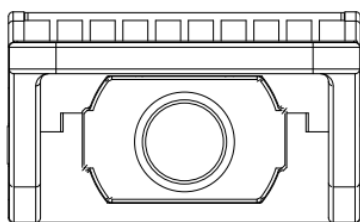
6. Programmable power consumption/burner

After power-up, the default power consumption is less than 8W to boot up the DSP, MCU and associated control logic/circuitry. Afterward, host can set the module to consume higher power by programming the 3 burners in 3 regions in section.

7. Status LED

A multi-color LED viewed from the front of the module in order to signify high/low power modes, module fully insert, and interrupts:

7.1 LED interface arrangement



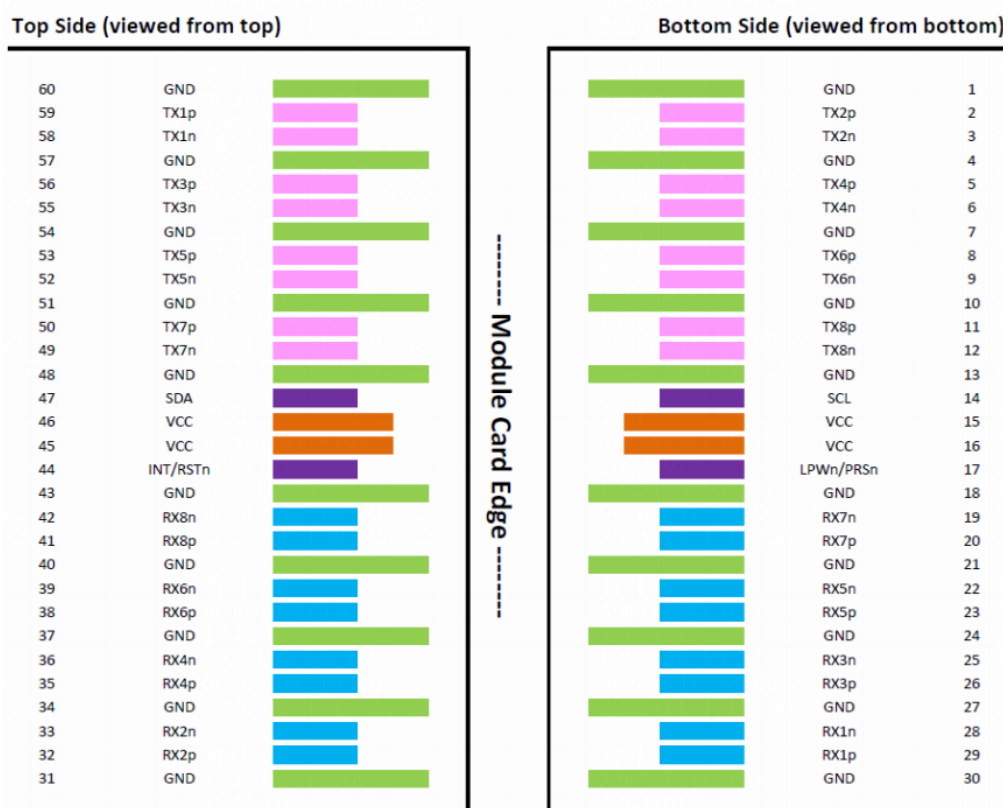
TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

7.2 Induction of Status Lights

LED	System state	Induction
Module status	Module is not powered on	OFF
	Module is operating in high power mode	Green (solid)
	Module is operating in low power mode	Orange (solid)
	Module in high pwer mode with voltage or temperature alarm	Green blinking
	Module in low power mode with voltage or temperature alarm	Orange blinking
	Module is in high temperature cut-off fault	Red blinking

8. Pin arrangement

8.1 Pin View



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8.2 4-Pin Function Definitions

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
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28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Inverted	CML-I	Input from Host	3

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	REVISION : 01	AUTHORIZED BY : Ian Chou
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57	GND		Ground		1
58	TX1n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Inverted	CML-I	Input from Host	3
60	GND		Ground		1

9. Memory Map

9.1 00LowPage Note

Page	Address	Size	Name	Description											
N/A	0	1	Identifier	19h: Identifier Type of OSFP											
	1	1	CmisRevision	53h: CMIS5.2 support											
	2	1	I2C speed	04h: Module supports up to 1 MHz											
	3	1	BIT:7-4 Reserved	Reserved											
			BIT:3-1 Module state	Current Module State: <table><tr><th>Code</th><th>Module State</th></tr><tr><td>001b</td><td>ModuleLowPwr</td></tr><tr><td>010b</td><td>ModulePwrUp</td></tr><tr><td>011b</td><td>ModuleReady</td></tr><tr><td>100b</td><td>ModulePwrDn</td></tr><tr><td>101b</td><td>ModuleFault</td></tr></table>	Code	Module State	001b	ModuleLowPwr	010b	ModulePwrUp	011b	ModuleReady	100b	ModulePwrDn	101b
Code	Module State														
001b	ModuleLowPwr														
010b	ModulePwrUp														
011b	ModuleReady														
100b	ModulePwrDn														
101b	ModuleFault														
		BIT:0 InterruptDeasserted	Status of Interrupt output signal 1b: Interrupt not asserted (default) 0b: Interrupt asserted												
	4	1	SumFlagBank0 BIT3: FlagsSummaryBank0Page2Ch	1b: at least one Flag is set on Bank 0, Page 2Ch											

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			BIT2: FlagsSummaryBank0Page14h BIT1: FlagsSummaryBank0Page12h BIT0: FlagsSummaryBank0Page11h	1b: at least one Flag is set on Bank 0, Page 14h 1b: at least one Flag is set on Bank 0, Page 12h 1b: at least one Flag is set on Bank 0, Page 11h
	8	1	BIT:6 CdbCmdCompleteFlag1 BIT:0 ModuleStateChangedFlag	Latched Flag to indicate completion of a CDB command for CDB instance 1. Latched Flag to indicate a Module State Change
	9	1	BIT:7 VccMonLowWarningFlag BIT:6 VccMonHighWarningFlag BIT:5 VccMonLowAlarmFlag BIT:4 VccMonHighAlarmFlag BIT:3 TempMonLowWarningFlag BIT:2 TempMonHighWarningFlag BIT:1 TempMonLowAlarmFlag BIT:0 TempMonHighAlarmFlag	Latched Flag for low/high supply voltage warning/alarm Latched Flag for low/high temperature warning/alarm
	12	2	TempMonValue 2	S16 Module Temperature Monitor (Current Value) internally measured temperature in 1/256 degree Celsius increments
	14	2	TempMonValue 1	S16 Module Temperature Monitor (Current Value) internally measured temperature in 1/256 degree Celsius increments
	16	2	VccMonVoltage	U16 Supply Voltage Monitor (Current Value) internally measured input supply voltage in 100 μ V increments

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	26	1	BIT:7 BankBroadcastEnable BIT:6 LowPwrAllowRequestHW BIT:4 LowPwrRequestSW BIT:3 SoftwareReset	0b: Bank broadcast for lane-banked pages disabled Enables evaluation of the LowPwrRequestHW hardware signal 0b: Module ignores the LowPwrRequestHW signal 1b: Module evaluates the LowPwrRequestHW signal (default) 0b: No request 1b: Request for the module to stay in, or to return into, Low Power mode Self-clearing trigger bit that causes the module to be reset when 1b is written to it. The effect of a SoftwareReset trigger is the same as asserting the Reset hardware signal for the appropriate hold time, followed by its de-assertion. 0b: No action 1b: Software reset (include all)
	31	1	BIT:6 CdbCmdCompleteMask1 BIT:2 DataPathFirmwareErrorMask BIT:1 ModuleFirmwareErrorMask	Mask bit for CdbCmdCompleteFlag1 Mask bit for DataPathFirmwareErrorFlag Mask bit for ModuleFirmwareErrorFlag

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			BIT:0 ModuleStateChangedMask	Mask bit for ModuleStateChangedFlag
32	1	BIT:7 VccMonLowWarningMask		Mask bit for VccMonLowWarningFlag
		BIT:6 VccMonHighWarningMask		Mask bit for VccMonHighWarningFlag
		BIT:5 VccMonLowAlarmMask		Mask bit for VccMonLowAlarmFlag
		BIT:4 VccMonHighAlarmMask		Mask bit for VccMonHighAlarmFlag
		BIT:3 TempMonLowWarningMask		Mask bit for TempMonLowWarningFlag
		BIT:2 TempMonHighWarningMask		Mask bit for TempMonHighWarningFlag
		BIT:1 TempMonLowAlarmMask		Mask bit for TempMonLowAlarmFlag
		BIT:0 TempMonHighAlarmMask		Mask bit for TempMonHighAlarmFlag
37	1	CdbStatus1		Refer CMIS 5.2
39	1	ModuleActiveFirmwareMajorRevision		0x00 U8 Numeric representation of the module 's active firmware major revision
40	1	ModuleActiveFirmwareMinorRevision		0x01 U8 Numeric representation of the module 's active firmware major revision
85	1	Module Type Encodings		0x03 Passive and Linear Active Copper Cables
86	1	ApSelCode 1: Host Electrical Interface Code		0x51 800GAUI-8 S C2M
87	1	ApSelCode 1: Module Media Interface Code		0xBF Passive Loopback module
88	1	ApSelCode 1: Host/Media Lane Count		0x80 Host Lane Count 8,and Media Lane Count 0
89	1	ApSelCode 1: Host Lane Assignment Options		0x01 Start Channel 1 for use this APP
90	1	ApSelCode 2: Host Electrical Interface Code		0x4F 400GAUI-4-S C2M

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91	1	ApSelCode 2: Module Media Interface Code	0xBF	Passive Loopback module
92	1	ApSelCode 2: Host/Media Lane Count	0x40	Host Lane Count 4,and Media Lane Count 0
93	1	ApSelCode 2: Host Lane Assignment Options	0x11	Start Channel 1 and 5 for use this APP
94	1	ApSelCode 3: Host Electrical Interface Code	0x52	800GAUI-8 L C2M
95	1	ApSelCode 3: Module Media Interface Code	0xBF	Passive Loopback module
96	1	ApSelCode 3: Host/Media Lane Count	0x80	Host Lane Count 8,and Media Lane Count 0
97	1	ApSelCode 3: Host Lane Assignment Options	0x01	Start Channel 1for use this APP
98	1	ApSelCode 4: Host Electrical Interface Code	0x50	400GAUI-4-S C2M
99	1	ApSelCode 4: Module Media Interface Code	0xBF	Passive Loopback module
100	1	ApSelCode 4: Host/Media Lane Count	0x40	Host Lane Count 4,and Media Lane Count 0
101	1	ApSelCode 4: Host Lane Assignment Options	0x11	Start Channel 1, 5 for use this APP
102	1	ApSelCode 5: Host Electrical Interface Code	0x4B	100GAUI-1-S
103	1	ApSelCode 5: Module Media Interface Code	0xBF	Passive Loopback module
104	1	ApSelCode 5: Host/Media Lane Count	0x10	Host Lane Count 1,and Media Lane Count 0
105	1	ApSelCode 5: Host Lane Assignment Options	0xFF	Start Channel 1,2,3,4,5,6,7,8 for use this APP
106	1	ApSelCode 6: Host Electrical Interface Code	0x4C	400GBASE-CR4
107	1	ApSelCode 6: Module Media Interface Code	0xBF	Passive Loopback module
108	1	ApSelCode 6: Host/Media Lane Count	0x10	Host Lane Count 1,and Media Lane Count 0
109	1	ApSelCode 6: Host Lane Assignment Options	0xFF	Start Channel 1,2,3,4,5,6,7,8 for use this APP
110	1	ApSelCode 7: Host Electrical Interface Code	0x11	400GAUI-8 C2M
111	1	ApSelCode 7: Module Media Interface Code	0xBF	Passive Loopback module
112	1	ApSelCode 7: Host/Media Lane Count	0x80	Host Lane Count 8,and Media Lane Count 0
113	1	ApSelCode 7: Host Lane Assignment Options	0x01	Start Channel 1 for use this APP
114	1	ApSelCode 8: Host Electrical Interface Code	0x0E	200GAUI-8 C2M
115	1	ApSelCode 8: Module Media Interface Code	0xBF	Passive Loopback module
116	1	ApSelCode 8:	0x80	Host Lane Count 8,and Media Lane Count 0

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
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	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

			Host/Media Lane Count	
	117	1	ApSelCode 8: Host Lane Assignment Options	0x01 Start Channel 1 for use this APP
	118-121	4	PasswordChangeEntryArea	U32: new password value
	122-125	4	PasswordEntryArea	U32: password value
	126	1	BankSelect	Refer CMIS 5.2
	127	1	PageSelect	Refer CMIS 5.2

9.2 00HighPage Note

Page	Address	Size	Name	Description
00h	128	1	Identifier	19h: Identifier Type of OSFP
	129-144	16	Vendor name	Vendor name (ASCII)
	145-147	3	VendorOUI	Vendor IEEE company ID
	148-163	16	VendorPN	Part number provided by vendor (ASCII)
	164-165	2	VendorRev	Revision level for part number provided by vendor (ASCII)
	166-181	16	VendorSN	Vendor Serial Number (ASCII)
	182-189	8	DateCode	Manufacturing Date Code (ASCII) Refer CMIS 5.2
	190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
	200	1	ModulePowerCtrl BIT:6 Region 3 burner Enable BIT:5 Region 2 burner Enable BIT:0 Region 5 burner Enable	BIT0, BIT5, and BIT6 control three heating blocks, with 1 turning heating on and 0 turning it off.
	201	1	MaxPower	0x54:MaxPower 21w(for adaptation switch)
	214	1	Region 3 power consumption	Set Value
	215	1	Region 2 power consumption	0x10
	218	1	Region 5 power consumption	0x18
				0x20
				0x28
				0x30

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
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				0x38	2.5
				0x40	3.0
				0x48	3.5
				0x50	4.0
				0x58	4.5
				0x60	5.0
				0x68	5.5
				0x70	6.0
				0x78	6.5
				0x80	7.0
				0x88	7.2
				0x90	8.0
				0x98	8.5
				0xA0	9.0
	222	1	page checksum	Refer CMIS 5.2	
	223-255	33	Custom Info	Refer CMIS 5.2	

9.3 01HighPage Note

Page	Address	Size	Name	Description
01h	128	1	ModuleInactiveFirmwareMajorRevision	0x00
	129	1	ModuleInactiveFirmwareMinorRevision	0x01
	130	1	ModuleHardwareMajorRevision	0x01
	131	1	ModuleHardwareMinorRevision	0x00
	142	1	BIT:6 VDMPagesSupported BIT:5 DiagnosticPagesSupported BIT:2 Page03hSupported BIT1-0: BanksSupported	1b : supported VDM page 20-2F 1b : DiagnosticPages13h-14h supported 1b : User Page 03h supported 00b: Bank 0 supported (8 lanes)
	144	1	Maximum duration of the DPDeinit / DPInit state	87h: DPDeinit : 5 s <= T state < 10 s DPInit : 1 s <= T state < 5 s
	145	1	BIT:7	

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			CoolingImplemented BIT:6-5 TxInputClockingCapabilities BIT:3 ePPSSupported BIT:3 TimingPage15hSupported BIT:2 Aux3MonObservable BIT:1 Aux2MonObservable BIT:0 Aux1MonObservable	Ob:Uncooled transmitter device 11b: Lanes may be asynchronous in frequency Ob: ePPS signal processing not supported Ob: Timing characteristics (Page 15h) not supported Ob: Aux 3 monitor monitors Laser Temperature Ob: Aux 2 monitor monitors Laser Temperature Ob: Aux 1 monitor is custom
	146	1	ModuleTempMax	5Ah: Maximum allowed module temperature 90°C
	147	1	ModuleTempMin	FBh: Maximum allowed module temperature -5°C
	150	1	OperatingVoltageMin	94h: Minimum supported module operating voltage 2.9V
	151	1	BIT:6-5 RxOutputEqType	00b: Peak-to-peak (p-p) amplitude stays constant, or not implemented, or no information
	153	1	BIT:7-4 RxOutputLevel 3-0 Supported BIT:3-0 TxInputEqMax	0Fh: Amplitude Code 3-0 supported 00h: TxInput Eq is Auto changed,No manual Eq Max value
	154	1	BIT:7-4 RxOutputEqPostCursorMax BIT:3-0 RxOutputEqPreCursorMax	0X07:Post-Cursor Equalization 7 dB 0X07:Pre-Cursor Equalization 3.5 dB
	155	1	BIT:0 InputPolarityFlipTxSupported	Ob:InputPolarityFlipTx control not supported
	156	1	BIT:7 BankBroadcastSupported	Ob: The BankBroadcastEnable control is not supported

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			BIT:2 AutoSquelchDisableRxSupported BIT:1 OutputDisableRxSupported BIT0:OutputPolarityFlipRxSupported	0b: Host cannot disable automatic squelching of Rx outputs using the AutoSquelchDisableRx register. 1b: Host can disable Rx outputs using the OutputDisableRx register 0b: PolarityFlipRx not supported
	157	1	BIT:1 LOSFlagTxSupported BIT:0 FailureFlagTxSupported	1b: Tx Loss of Signal Flags supported 1b: Tx Fault Flags supported
	159	1	BIT:5 CustomMonSupported BIT:4 Aux3MonSupported BIT:3 Aux2MonSupported BIT:2 Aux1MonSupported BIT:1 VccMonSupported BIT:0 TempMonSupported	1b: Custom monitor supported 0b: Aux 3 monitor not supported 0b: Aux 2 monitor not supported 0b: Aux 1 monitor not supported 1b: Internal 3.3 V monitor supported 1b: Temperature monitor supported
	161	1	BIT:6-5 TxInputEqRecallBuffersSupported BIT:4 TxInputEqFreezeSupported BIT:3 TxInputAdaptiveEqSupported BIT:2 TxInputEqHostControlSupported BIT:1 TxCDRBypassControlSupported	00b: Tx Input Eq Store/Recall not supported 0b: Tx Input Eq Freeze not supported 1b: Adaptive Tx Input Eq supported 0b: host-control of Tx Input Eq target not supported

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
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			BIT:0 TxCDRSupported	0b: If a Tx CDR is supported, it cannot be bypassed 1b: Tx CDR supported supported
162	1		BIT:7 VersatileControlSetSupported BIT:6 UnidirReconfigSupported BIT:5 StagedSet1Supported BIT:4-3 RxOutputEqControlSupported BIT:2 RxOutputAmplitudeControlSupported BIT:1 RxCDRBypassControlSupported BIT:0 RxCDRSupported	0b: CMIS-VCS [6] functionality is not supported 0b: ApplyImmediateTx/Rx on Page 10h and DPConfigTx/Rx on Page 19h are not supported 1b:Staged Control Set 1 supported on Page 10h 11b: both Pre- and Post-cursor supported 1b: Rx Output Amplitude control supported 0b: Rx CDR Bypass control not supported (if a CDR is supported, it cannot be bypassed) 1b: Rx CDR supported
163	1		CDB Advertisement	0x67: Refer CMIS 5.2 for detail
164	1		CdbReadWriteLengthExtension	0xFF:Refer CMIS 5.2 for detail
165	1		CdbCommandTriggerMethod,and CdbExtMaxBusyTime	0x9F:Refer CMIS 5.2 for detail
166	1		CdbMaxBusySpecMethod , CdbMaxBusyTime	0x80:Refer CMIS 5.2 for detail
167	1		BIT:7-4: MaxDurationModulePwrDn BIT:3-0 MaxDurationModulePwrUp	0X06: 500 ms <= T state < 1 s 0X08: 5 s <= T state < 10 s
168	1		BIT:7-4: MaxDurationDPTxTurnOff BIT:3-0 MaxDurationDPTxTurnOn	0X05: 100 ms <= T state < 500 ms 0X07: 1 s <= T state < 5 s
223	1		ApSelCode 9: Host Electrical Interface Code	0x0A: 50GAUI-1 C2M
224	1		ApSelCode 9: Module Media Interface Code	0xBF: Passive Loopback module

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

	225	1	ApSelCode 9: Host/Media Lane Count	0x10: Host Lane Count 1,and Media Lane Count 0
	226	1	ApSelCode 9: Host Lane Assignment Options	0xFF: Start Channel 1,2,3,4,5,6,7,8 for use this APP
	227	1	ApSelCode 10: Host Electrical Interface Code	0x05: CAUI-4 C2M(Annex83E)
	228	1	ApSelCode 10: Module Media Interface Code	0xBF: Passive Loopback module
	229	1	ApSelCode 10: Host/Media Lane Count	0x10: Host Lane Count 1,and Media Lane Count 0
	230	1	ApSelCode 10: Host Lane Assignment Options	0xFF: Start Channel 1,2,3,4,5,6,7,8for use this APP
	231	1	ApSelCode 11: Host Electrical Interface Code	0x41: CAUI-4 C2M(Annex83E)
	232	1	ApSelCode 11: Module Media Interface Code	0xBF: Passive Loopback module
	233	1	ApSelCode 11: Host/Media Lane Count	0x40: Host Lane Count 4,and Media Lane Count 0
	234	1	ApSelCode 11: Host Lane Assignment Options	0x11: Start Channel 1,5for use this APP
	235	1	ApSelCode 12: Host Electrical Interface Code	0xFF: FFh to mark as unused (empty Application Descriptor)
	255	1	Page Checksum	The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 130 to byte 254, inclusive

9.4 02 HighPage Note

Page	Address	Size	Name	Description
02h	128-129	2	TempMonHighAlarmThreshold	0x5A00: Temp High Alarm 90℃
	130-131	2	TempMonLowAlarmThreshold	0xF600: Temp Low Alarm -10℃
	132-133	2	TempMonHighWarningThreshold	0x5500: Temp High Warning 85℃
	134-135	2	TempMonLowWarningThreshold	0xFB00: Temp Low Warning -5℃
	136-137	2	VccMonHighAlarmThreshold	0x8DCC: Vcc High Alarm 3.63V
	138-139	2	VccMonLowAlarmThreshold	0x7404: Vcc Low Alarm 2.97V
	140-141	2	VccMonHighWarningThreshold	0x875A: Vcc High Warning 3.47V
	142-143	2	VccMonLowWarningThreshold	0x7A76: Vcc High Warning 3.14V

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

9.5 03 HighPage Note

Page	Address	Size	Name	Description
03h	128-255	128	User Data	Module user data stored in NV memory
	129	1	BIT:7-4 Green Led Status BIT:3-0 Red Led Status	Current LED Status 0000b: Off 0001b:On 00010:Blinking
	138	1	Heater Time Set(Minute)	Set heater time
	139	1	BIT:5 LpMod Control BIT1: LPWn logic status	Read 0b:No edge detected Read 1b:Either rising edge or falling edge crossing the 1.25V thrshold is detected. Write 0b: No effect Write1b: clear the Bit Read 1b: High Read 0b: Low
	140	1	BIT:1-0 INTL control	0xb:Normal Operation 10b:Force M_INT to logic 0 11b:Force M_INT to logic 1
	168	2	Supply Volatge Size on VccTx	
	170	2	Supply Volatge Size on VccRx	
	174	2	Supply Current Size on VccTx	
	176	2	Supply Current Size on VccRx	
	182	2	Dsp Version	(ASCII) RO

9.6 10 HighPage Note

Page	Address	Size	Name	Description
10h	128	1	Data Path initialization control	Refer CMIS5.2
	138	1	OutputDisableRx<i>	0b: Rx output enabled for lane <i> 1b: Rx output disabled for lane <i>
	143	1	SCS0::ApplyDPInitLane<i>	Refer CMIS5.2
	144	1	SCS0::ApplyImmediate<i>	Refer CMIS5.2
	145-152	8	SCS0::DPConfigLane1-8	Refer CMIS5.2

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

	162-165	4	SCS0::OutputEqPreCursorTargetRx<i>	Refer CMIS5.2
	166-169	4	SCS0::OutputEqPostCursorTargetRx<i>	Refer CMIS5.2
	170-173	4	SCS0::OutputAmplitudeTargetRx<i>	Refer CMIS5.2
	176	1	SCS0::ApplyImmediateTx<i>	Refer CMIS5.2
	177	1	SCS0::ApplyImmediateRx<i>	Refer CMIS5.2
	178	1	SCS1::ApplyDPInitLane<i>	Refer CMIS5.2
	179	1	SCS1::ApplyImmediate<i>	Refer CMIS5.2
	180-187	8	SCS1::DPConfigLane1 -8	Refer CMIS5.2
	197-200	4	SCS1::OutputEqPreCursorTargetRx<i>	Refer CMIS5.2
	201-204	4	SCS1::OutputEqPostCursorTargetRx<i>	Refer CMIS5.2
	205-208	4	SCS1::OutputAmplitudeTargetRx<i>	Refer CMIS5.2
	211	1	SCS1::ApplyImmediateTx<i>	Refer CMIS5.2
	212	2	SCS1::ApplyImmediateRx<i>	Refer CMIS5.2
	213	1	DPStateChangedMask<i>	Refer CMIS5.2
	215	1	LOSMaskTx<i>	Refer CMIS5.2
	216	1	CDRLOLMaskTx<i>	Refer CMIS5.2
	232	1	OutputStatusChangedMaskRx<i>	Refer CMIS5.2

9.7 11 HighPage Note

Page	Address	Size	Name	Description
11h	128-131	4	Data Path States	Refer CMIS5.2
	132	1	OutputStatusRx<i>	Refer CMIS5.2
	134	1	DPStateChangedFlag<i>	Refer CMIS5.2
	136	1	LOSFlagTx<i>	Refer CMIS5.2
	137	1	CDRLOLFlagTx<i>	Refer CMIS5.2
	153	1	OutputStatusChangedFlagRx<i>	Refer CMIS5.2
	202-205	4	ConfigStatusLane<i>	Refer CMIS5.2
	206-213	8	ACS::DPConfigLane1-8	Refer CMIS5.2
	223-226	4	ACS::OutputEqPreCursorTargetRx<i>	Refer CMIS5.2

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

	227-230	4	ACS::OutputEqPostCursorTargetRx<i>	Refer CMIS5.2
	231-234	4	ACS::OutputAmplitudeTargetRx<i>	Refer CMIS5.2

9.8 13 HighPage Note

Page	Address	Size	Name	Description
13h	128	1	Loopback capabilities	0X08: HostSideInputLoopback
	129	1	BIT:7-6 GatingSupport BIT:5 GatingResultsSupported BIT:4 PeriodicUpdatesSupported BIT:3 PerLaneGatingTimersSupported BIT:2 AutoRestartGatingSupported	11b: Supported with time accuracy > 20 ms 1b: Supported 1b: periodic update during measurement 0b: Only two global gating timers are available for all lanes on all Banks, one for Host Side Measurements and one for Media Side Measurements. 1b: AutoRestartGating control (13h:177.4) supported
	130	1	BIT:6 HostSideFEC BIT:4 HostSideInputSNRMeasurement BIT:1 BitsAndErrorsCountingSupported BIT:0 BitErrorRatioResultsSupported	1b: Supported (PRBS error information available) 1b: Supported 1b: Supported 1b: Supported
	131	1	BIT:2 PRBSGeneratorHostSidePostFEC	

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

			BIT:0 PRBSCheckerHostSidePostFEC	1b: Supported 1b: Supported
	132-133	2	HostSideGeneratorSupportsPattern<i>	0XFF0A Refer CMIS5.2
	136-137	2	HostSideCheckerSupportsPattern<i>	0XFF1F Refer CMIS5.2
	141	1	BIT:3 HostSideCheckerSupportsDataSwap BIT:2 HostSideCheckerSupportsDataInvert BIT:1 HostSideGeneratorSupportsDataSwap BIT:0 HostSideGeneratorSupportsDataInvert	0b: not supported 1b: supported 0b: not supported 0b: not supported
	142	1	BIT:3 HostCheckerSupportsPerLaneEnable BIT:2 HostCheckerSupportsPerLanePattern BIT:1 HostGeneratorSupportsPerLaneEnable BIT:0 HostGeneratorSupportsPerLanePattern	1b: per lane enable supported 1b: per lane enable supported 1b: per lane enable supported 1b: per lane enable supported
	144	1	HostSideGeneratorEnableLanex	Refer CMIS5.2
	148-151	4	HostSideGeneratorPatternSelectLanex	Refer CMIS5.2
	160	1	HostSideCheckerEnableLanex	Refer CMIS5.2
	161	1	HostSideCheckerDataInvertLanex	Refer CMIS5.2
	164-167	1	HostSideCheckerPatternSelectLanex	Refer CMIS5.2

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

	176	1	HostPRBSGeneratorClockSource	0b: All lanes use Internal Clock
	177	1	BIT:7 StartStopsGlobal BIT:5 ResetErrorInformation BIT:4 AutoRestartGating BIT:3-1 MeasurementTime BIT:0 UpdatePeriodSelect	0b: A start/stop control change acts on current Bank Refer CMIS5.2 Refer CMIS5.2 Refer CMIS5.2 Refer CMIS5.2
	208	1	PatternCheckGatingCompleteMaskHostLane<i>	Refer CMIS5.2
	212	1	PatternCheckerLOLMaskHostLane<i>	Refer CMIS5.2

9.9 14 HighPage Note

Page	Address	Size	Name	Description
14h	128	1	DiagnosticsSelector	Refer CMIS5.2 Supported by 01h,02h,03h,06h
	134	1	PatternCheckGatingCompleteFlagHostLane<i>	Refer CMIS5.2
	138	1	PatternCheckerLOLFlagHostLane<i>	Refer CMIS5.2
	192-255	64	Diagnostics Data	Refer CMIS5.2

9.10 20HighPage Note

Page	Address	Size	Name	Description
20h	128-143	16	VDMDescriptor (Defaule Set SNR (dB) Host Input (Lane 1-8))	Refer CMIS5.2
	144-159	16	VDMDescriptor (Defaule Set PAM4 Level Transition Parameter Host Input (Lane 1-8))	Refer CMIS5.2

TITLE 800G OSFP-IHS Active Loopback Module	DOC No.NRFD-20260521100-002	
	REVISION : 01	AUTHORIZED BY : Ian Chou
	DATE : 2026.05.21	CLASSIFICATION : Optical Transceiver

9.11 24HighPage Note

Page	Address	Size	Name	Description
24h	128-143	16	eSNR Host Input (Host Lane 1-8)	RO
	144-159	16	PAM4 LTPM Input (Host Lane 1-8)	RO

9.12 2FHighPage Note

Page	Address	Size	Name	Description
2Fh	128	1	BIT:1-0 VDMSupport	0b: Group 1 (Page 20h, 24h, 28h, first ¼ of 2Ch, 2Dh)
	129-130	1	FineIntervalLength	0xC350:interval is 5s

9.13 FFHighPage Note

Page	Address	Size	Name	Description
FFh	250	2	Power-cycle counter	Power-cycle counter. Default to 00_00h from factory.

10. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026/05/21	Ian Chou	Mike Sun